A Simple Circuit Approach to Improve Speed and Power Consumption in Pulse-Triggered Flip-Flops

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In this paper, simple circuital techniques to design efficient pulse triggered flip-flops are presented. The proposed approach aims at considerably alleviating the detrimental effects of current contention mechanisms, occurring at critical switching nodes of the circuits. In this way, both latency and power consumption of pulse triggered flip-flops are reduced. The proposed approach is assessed by means of simulations in 90-nm ST commercial CMOS technology. When applied to some recently proposed implicit pulse triggered flip-flop architectures, the suggested design strategy, allows speed to be improved up to 13% and power-delay-product to be lowered down to 14%. Moreover, also the process variation tolerance is considerably improved.

Keywords: Flip-Flop, Low-Power, Pulse-Triggered.

1. INTRODUCTION

It is well known that choosing the appropriate flip flop (FF) topology is of fundamental importance in the design of synchronous digital systems (such as microprocessors). From a timing perspective, FF latency consumes a large portion of the clock cycle time while the operating frequency increases. Moreover, in order to sustain the trend of high performance and throughput, a large number of FFs is usually employed for extensive pipelining of datapath sections, causing the power dissipation of FFs having a deep impact on the power characteristics of the whole system.

Both master–slave (MS-) and pulsed-triggered (P-) FFs are commonly used in contemporary digital systems. Conventional MS-FFs consist of two latches called master and slave, respectively. These FFs are characterized by a positive setup time requirement that increases the data-to-output delay. P-FFs are considered to be an interesting alternative to MS-FFs. Their functioning is based on the generation of a narrow transparency window in correspondence of the rising (or falling) clock edge. In this way a near to zero or even negative setup time is allowed and smaller data-to-output delay is achieved. Moreover, since the operation of a P-FF requires only a single latch, as opposed to two latches needed in conventional MS configurations, the logic complexity and the number of stages of the circuit are reduced, thus leading to lower power consumption.

Depending on the method used to generate the transparency window, P-FFs are classified into two categories: the explicit P-FFs (EP-FFs) and the implicit P-FFs (IP-FFs). In EP-FFs, an external pulse generator circuit is exploited to generate the pulse signal, thus triggering the transparency window for the latching structure. A single pulse generator could be shared among neighboring latches, as in the Itanium 2 microprocessor. As an advantage of this solution, the power overhead of the pulse generator is distributed across many FFs, but, due to the increased capacitive load, the generation of a precisely timed pulse signal could be difficult to be managed in practice. Such an issue is further complicated in presence of process and environmental variations.

IP-FFs allow to eliminate the need to distribute the pulse signal by incorporating the pulse generator into their structures. In this way better control of transparency window width is enabled (so that a very narrow transparency window can be produced), usually at the expense of some speed penalties in comparison to EP-FF structures.

In the following, we will mainly focus on the design of IP-FFs. A design solution to achieve faster and lower power consuming IP-FFs is here proposed. When applied to some state-of-the-art IP-FF circuits, the proposed approach leads to reduce data-to-output delay from 8% to 13% and power-delay-product (PDP) from 10% to 14%,
while assuring the lowest power consumption for different input data signal switching activities and without any significant loss in terms of occupied silicon area. Moreover, the suggested circuit modifications lead to obtain higher process variation tolerance in terms of delay and PDP parameters.

The remainder of this paper is organized as follows: Section 2 surveys recently proposed low-power and high-speed IP-FFs. Section 3 suggests simple circuit techniques to increase speed and reducing power consumption of IP-FFs. Section 4 deals with comparative evaluations, performed exploiting the commercial 90 nm ST Microelectronics CMOS technology. Finally, Section 5 concludes the paper.

2. IMPLICIT PULSED FLIP FLOPS

Figure 1(a) shows the single-ended conditional capturing energy recovery (SCCER) IP-FF. The circuit mainly consists of two branches, sharing two clocked transistors (N1–N2) in their discharging paths, and a simple latch (P3/N6–P4/N7) which preserves the output signal (Q) while the FF is insensitive to the input data signal (D). The left branch of the circuit is responsible for capturing the high logic value of the input data signal, whereas the low logic value of D is captured by the right branch. The actual latching occurs only during the 1–1 overlap between CLK and CLKB signals. After the rising edge of CLK and before CLKB falls low, N1 and N2 are simultaneously turned on for a short period of time, thus triggering the FF transparency window. To save power, the SCCER design exploits the conditional capturing technique. This is implemented by using the feedback signal Q_fdbk to control the N3 transistor. Only when Q is low (i.e., Q_fdbk is high), a high logic value on the input signal D causes node X to be discharged during the FF transparency window. This in turn leads Q (Q_fdbk) to change from the low (high) to the high (low) logic value and, consequently, N3 to be turned off. As a result, node X is prevented from discharging in succeeding clock cycles as long as D is stable at the high logic value. In this way precious power can be saved.

As highlighted in Figure 1(a), the worst case delay of the SCCER design occurs when the output signal Q undergoes a low-to-high transition. In such a condition, node X has to be discharged through four stacked transistors (N1–N4) which have to win the contention with the always “on” pull-up transistor P1. A proper sized pull-down circuitry is thus needed to ensure that node X can be properly discharged. This implies the use of large N1–N4 devices and/or weak inverter I1 to widen the transparency window. However, sizing of the N1–N4 transistors is constrained by robustness issues. When most of the devices in the left branch discharging path become ON simultaneously, significant charge sharing may occur. In an extreme case, this can lead to an unwanted switching of the output signal outside the FF transparency window. Upsizing P1 helps in reducing the effect of charge sharing but, at the same time, increases the current contention at node X, when it has to be discharged. Indeed, the preferred option is to use minimum-sized pull-up PMOS (thus reducing the adverse impact on FF speed/power), while avoiding too large transistors in the pull-down path to guarantee a proper level of immunity to charge sharing effects.

As X is discharged, P2 is turned on, thus charging node Q at the VDD voltage level. However, because the NMOS N7 does not turn off instantaneously, there is another current contention mechanism occurring between P2 and N7 (due to the crossbar current flowing through P2 and N7) during the low-to-high transition of the output signal Q. Also such mechanism causes FF delay and power dissipation to be degraded.

The low-power conditional pulse enhanced FF (CPEFF), proposed by Hwang et al. is shown in Figure 1(b). A pseudo-explicit pulse generator, consisting of an inverter (I1) and a two-input pass transistor logic (PTL)-based AND gate, is used to trigger the FF transparency window. Such circuitry produces a diminished voltage swing pulse

![Fig. 1. Previous proposed implicit pulse-triggered flip-flops: (a) SCCER; (b) CPEFF; (c) CPSFF](image-url)
signal which reduces the switching power at node $Z$.\(^7\) Only when $X$ is discharging, the pulse signal at node $Z$ is raised to the $V_{DD}$ voltage level through $P3$, thus enhancing strength of transistor $N1$. Such clocking mechanism allows reducing the number of stacked NMOS devices in the left branch but, as a counter effect, a larger NMOS device (i.e., $N4$) is needed on the discharging path of the right branch to compensate the weakened action of transistor $N1$ during the capturing of the low logic value on the input signal $D$. Note that also the CPEFF suffers from the current contention drawbacks already described for the SCCER design.

The solution proposed by Zhao et al.\(^9\) preserves the simple clocking structure of the SCCER design and exploits the conditional data mapping technique\(^10\) to control the discharge path of the left branch of the circuit. The resulting FF, called clocked pair shared FF (CPSFF),\(^9\) is shown in Figure 1(c). On the basis of the $D$, $Q$ and $Q_{\text{fbk}}$ signals, the conditional data mapper switches off the discharge path of the left branch when a high logic value has to be maintained on the output. This avoids redundant transitions at node $X$ while the height of the NMOS stack in the left branch of the circuit is reduced. Unfortunately, the current contention at node $X$ and the crossbar current, occurring at the beginning of the low-to-high output signal transition, continue to negatively impact on speed and power of the CPSFF design.

In this work, the SCCER, CPEFF and CPSFF circuits, later used as the reference designs for the comparative analysis described in Section 4, were optimized with the objective of achieving a tradeoff between power consumption and $D$-to-$Q$bar delay i.e., minimizing the product of the two terms. Sizes of the devices belonging to the reference circuits are reported in Figures 1(a)–(c). There, channel widths are normalized to the minimum value $W_{\text{min}} (=0.12\ \text{um})$ imposed by the 90 nm ST Microelectronics CMOS technology. Where not indicated, devices were sized with minimum channel length $L_{\text{min}} (=0.1\ \text{um})$.

### 3. PROPOSED DESIGN APPROACH

In this section, some circuital modifications are suggested to alleviate the effects of current contention mechanisms occurring during the worst-case output switching of IP-FFs. Figure 2(a) illustrates the proposed design strategy when applied to the SCCER circuit. As clarified in the following, the same approach can be profitably used also for all the other circuits described in Section 2.

The contention reduced (CR)-SCCER circuit of Figure 2(a), replaces the always “on” pull-up transistor of the left branch with a parallel pull-up PMOS network ($P1$–$P5$) driven by feedback signals $Q$ and $Q_{\text{fbk}}$. In this way, the node $X$ is correctly maintained at $V_{DD}$ when the FF is not transparent to the data input, whereas current contention at node $X$ is reduced when it has to be discharged, during the FF transparency window. In fact, if a rising transition of the output signal has to occur (i.e., as a consequence of a rising transition of the input data signal which has to be captured during the FF transparency window), the discharge of the node $X$, determined by the pull-down network of the left branch, is counteracted by the charging current flowing through $P1$ only at the beginning of the falling transition of node $X$. As $X$ is lowered below the $V_{DD} - |V_{th, P2}|$ voltage level, $P2$ is turned on and $Q$ voltage starts to rise towards $V_{DD}$. As a consequence, the source to gate voltage ($V_{gs, P1}$) of $P1$ is gradually reduced, thus weakening the action of the device $P1$. Due to the delay introduced by the inverter $P3/N6$, $P1$ is completely switched off while $P5$ is not yet turned on. This means that there is a portion of time, during the FF transparency window, where no charging current is flowing through the pull-up network of the left branch. As a result the “fighting” problem at node $X$ results greatly alleviated with a positive impact on the switching speed of node $Q$. Additionally, the rising transition of node $Q$ is favored by the NMOS transistor $N8$ added in the pull-down network of the inverter $P4/N7$. Such device, controlled by node $X$, allows the NMOS pull-down network $N7$–$N8$, to be quickly turned off. In this way, the crossbar current flowing...

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**Fig. 2.** Contention reduced implicit pulse-triggered flip-flops: (a) CR-SCCER; (b) CR-CPEFF; (c) CR-CPSFF.
A Simple Circuit Approach to Improve Speed and Power Consumption in Pulse-Triggered Flip-Flops

Lanuzza

through $P2$ and $N7$–$N8$ is quickly zeroed with benefit in terms of charging speed for node $Q$. It is worth noting that, since current contentions are considerably reduced during the critical output switching, the suggested approach also results beneficial in terms of power dissipation, especially when the critical path delay is highly solicited (i.e., for high input data activities).

Figures 2(b)–(c) show the contention reduced versions of the CPEFF and CPSFF designs, respectively. In order to provide a direct evaluation of the impact of the proposed design approach, the original pull-down transistor sizing was maintained. Instead, the pull-up PMOS devices belonging to the left branch of the circuits were sized for 1.2 $W_{min}$ to assure robustness against charge sharing effects similar to that of the original designs. The additional NMOS device driven by node $X$ was sized with minimum channel width.

Note that the suggested design strategy leads to increase the capacitive loads on node $X$, $Q$ and $Q_{\text{fbk}}$. However, the speed advantages brought by the temporary switching off of the pull-up network of the left branch, when $X$ is discharging during the FF transparency window, greatly overcome the adverse impact of the increased parasitic capacitances on node $X$. Moreover, the devices, controlled by nodes $Q$ and $Q_{\text{fbk}}$, have minimal impact on the capacitive load of such nodes due their reduced sizing. Given all, the suggested approach leads to improve the overall speed and power consumption of the CR-FF designs.

4. COMPARATIVE RESULTS

The Cadence Spectre tool was employed for comparative analysis exploiting the simulation setup shown in Figure 3. In order to obtain accurate results, IP-FFs were simulated considering a realistic environment, where input buffers drive the FF inputs (CLK and $D$), and the outputs ($Q$ and $Q_{\text{bar}}$) drive a 20 fF load capacitance. An extra capacitance of 3 fF is placed after the clock driver. The clock frequency was set to 500 MHz, whereas the power supply voltage is 1 V.

The characteristics of the analyzed IP-FFs are compared in Table I in terms of total gate area, optimum setup time, hold time, $D$-to-$Q_{\text{bar}}$ delay, power consumption for different input data activities and PDP evaluated as the product between the $D$-to-$Q_{\text{bar}}$ delay and power for 50% input activity. Although the proposed approach requires two additional devices, the total gate area increasing of the CR-FF designs results to be negligible. Optimum setup-time is the setup time that minimizes the $D$-to-$Q_{\text{bar}}$ delay.

Mainly due to the increased capacitive loading on node $X$, the CR-FFs have the optimum setup time slightly increased (about 5 ps) in comparison to their conventional counterparts.

The CPEFF and the CR-CPEFF designs have hold time longer than other designs. This is because the pulse enhancement mechanism requires a more prolonged availability of the input data signal. The SCCER and CPSFF circuits shorten the hold time of about 43% and 48% with respect the CPEFF design. Anyway, when compared to their conventional counterparts, the CR-FFs always reduce hold time requirements.

Due to the reduced current contentions during the worst-case output switching, all the CR-FFs shorten the $D$-to-$Q_{\text{bar}}$ delay in comparison to their conventional counterparts. More precisely, at the optimum setup time, CR-SCCER, CR-CPEFF and CR-CPSFF designs improve $D$-to-$Q_{\text{bar}}$ delay of about 10%, 13% and 8% when compared to SCCER, CPEFF and CPSFF circuits, respectively.

As shown in Figure 4, such speed advantage is maintained for different setup times. Even though the optimum setup time of the CR-FFs is slightly increased in comparison to that of their conventional counterparts, the CR-FFs retain the ability to work correctly for negative setup times. This provides soft-clock edge property for overcoming clock skew related cycle time loss. Therefore, the CR-FFs present proper timing characteristics for high-performance applications.

As the power dissipated in a FF depends on input data activities, five different input patterns were considered to evaluate the power consumption behavior of the compared designs. The considered patterns present 0% (all-zero or all-one), 25%, 50%, and 100% data transition probabilities, respectively. Both the clock buffer power and total power dissipation in the proposed approach is lower than the original counterparts.
power (including power consumed in the latches and in the data and clock drivers) data are reported in Table I. Again, reduced current contentions, lead the CR-FFs to achieve slightly better power results in comparison to their conventional counterparts, especially for the highest input data activities. It is worth noting that, if power becomes the primary concern, the increased speed, brought by the suggested design approach, could be traded-off for additional power saving by reducing sizing of pull-down devices in the left branch of the CR-FF circuits.

Due to the improved power and timing characteristics, the CR-FFs achieve significantly better PDP results in comparison to the previous proposed designs. Figure 5 illustrates the curves of PDP versus setup time. At the optimum setup time, CR-SCCER, CR-CPEFF and CR-CPSFF reduce the PDP of about 13%, 14% and 10% when compared to SCCER, CPEFF and CPSFF, respectively. Therefore, the CR-FFs are confirmed to be a good design option for low-power and high-performance applications.

Table II gives the leakage power of all FF designs in standby mode [nW]. (CLK,D,Q)/ IP-FF SCCER\(^1\) CR-SCCER CPEFF\(^3\) CR-CPEFF CPSFF\(^9\) CR-CPSFF

<table>
<thead>
<tr>
<th>Num of trans./tot. gate area [um(^2)]</th>
<th>171/1.493</th>
<th>19/1.522</th>
<th>19/1.458</th>
<th>21/1.487</th>
<th>19/1.589</th>
<th>21/1.618</th>
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<tr>
<td>Optimum setup time [ps]</td>
<td>0</td>
<td>5</td>
<td>–15</td>
<td>–10</td>
<td>–5</td>
<td>0</td>
</tr>
<tr>
<td>Hold time [ps]</td>
<td>60</td>
<td>35</td>
<td>105</td>
<td>100</td>
<td>55</td>
<td>30</td>
</tr>
<tr>
<td>Min. data to Qbar delay [ps]</td>
<td>125.9</td>
<td>113.1</td>
<td>132</td>
<td>115.4</td>
<td>127.4</td>
<td>117</td>
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<tr>
<td>Clock buffer power [uW]</td>
<td>9.7</td>
<td>9.7</td>
<td>10.7</td>
<td>10.7</td>
<td>9.6</td>
<td>9.6</td>
</tr>
<tr>
<td>Power (100% activity) [uW]</td>
<td>29.4</td>
<td>28</td>
<td>30.7</td>
<td>29.8</td>
<td>29.2</td>
<td>28.2</td>
</tr>
<tr>
<td>Power (50% activity) [uW]</td>
<td>21.2</td>
<td>20.6</td>
<td>22</td>
<td>21.5</td>
<td>21.1</td>
<td>20.6</td>
</tr>
<tr>
<td>Power (25% activity) [uW]</td>
<td>17.2</td>
<td>16.9</td>
<td>17.6</td>
<td>17.4</td>
<td>17.1</td>
<td>16.8</td>
</tr>
<tr>
<td>Power (0% all-one) [uW]</td>
<td>15.3</td>
<td>15.1</td>
<td>15.5</td>
<td>15.3</td>
<td>15.4</td>
<td>15.2</td>
</tr>
<tr>
<td>Power (0% all-zero) [uW]</td>
<td>14.8</td>
<td>14.8</td>
<td>15.1</td>
<td>15.1</td>
<td>14.6</td>
<td>14.6</td>
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<tr>
<td>Power-delay-product (50% activity) [nJ]</td>
<td>2.66</td>
<td>2.33</td>
<td>2.87</td>
<td>2.47</td>
<td>2.69</td>
<td>2.42</td>
</tr>
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</table>

Table II. Leakage power consumption in standby mode [uW].

process corners. It is easy to observe that the speed advantages of the CR-FFs are maintained quite constant over the different process corners, except for the SS corner case where no significant speed improvements were observed. As shown in Figure 7, a similar behavior was observed in terms of PDP.

Pulsed FFs are usually very sensitive to random process variability.\(^{13,14}\) For this reason, the tolerance to process uncertainties was analyzed for all the compared circuits. Figures 8(a)–(c) illustrate the PDP versus the D-to-Qbar delay spreads obtained from a 1000-point Monte-Carlo simulation, performed considering both inter-die and

![Fig. 5.](image5.png)  
**Fig. 5.** PDP versus setup time for the compared flip-flops.

![Fig. 6.](image6.png)  
**Fig. 6.** D-to-Qbar delay at different process corners.
A Simple Circuit Approach to Improve Speed and Power Consumption in Pulse-Triggered Flip-Flops

Lanuzza

Fig. 7. PDP at different process corners (50% activity).

Table III. Monte Carlo results.

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<tbody>
<tr>
<td>Data to Qbar delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\mu$ [ps]</td>
<td>125.5</td>
<td>110.7</td>
<td>132</td>
<td>115.5</td>
</tr>
<tr>
<td>$\sigma$ [ps]</td>
<td>10.8</td>
<td>9.17</td>
<td>11.6</td>
<td>9.6</td>
</tr>
<tr>
<td>PDP (50% activity)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\mu$ [fJ]</td>
<td>2.67</td>
<td>2.29</td>
<td>2.89</td>
<td>2.47</td>
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<tr>
<td>$\sigma$ [fJ]</td>
<td>0.24</td>
<td>0.19</td>
<td>0.26</td>
<td>0.21</td>
</tr>
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</table>

intra-die variations. In this analysis, FFs operate at their optimum setup time (see Table I), without any setup time margin. In Table III, mean ($\mu$) and standard deviation ($\sigma$) values are reported for the $D$-to-Qbar delay and PDP, respectively. As expected, the suggested approach, lead the CR-FFs to achieve better mean $D$-to-Qbar delay and PDP with respect their conventional counterparts. The reduced current contentions during the worst-case output switching, lead the CR-FFs also to achieve higher process variation tolerance. This is confirmed by observing standard deviation ($\sigma$) values for the $D$-to-Qbar delay and PDP, which result considerably reduced. More precisely, the reduction of $\sigma_{\text{Delay}}$ ranges between 13% (CR-CPSFF vs. CPSFF) and 17% (CR-CPEFF vs. CPEFF). At the same time, the reduction of $\sigma_{\text{PDP}}$ is between 15% (CR-CPSFF vs. CPSFF) and 20% (CR-CPEFF vs. CPEFF).

5. CONCLUSION

State-of-the-art implicit pulsed flip-flops suffer from current contentions occurring at critical switching nodes when the worst-case delay path is solicited. This has an adverse impact on data-to-output delay and power consumption of the circuits. In this paper, simple circuital techniques to considerably alleviate the detrimental effects of current contentions, occurring during the worst-case output switching, are proposed. When applied to state-of-the-art implicit pulse triggered flip-flops, the suggested approach allows data-to-output delay to be improved up to 13% and power-delay-product to be reduced down to 14%, without any significant penalty in terms of occupied silicon area. Moreover, the reduced current contentions, lead to improve process variation tolerance of the modified designs. Interestingly, the suggested approach can be easily mixed with several low power techniques, including low swing and double edge clocking, to design more effective pulse-triggered flip-flops.

References

A Simple Circuit Approach to Improve Speed and Power Consumption in Pulse-Triggered Flip-Flops


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Marco Lanuzza received the M.Sc. degree in Electronic Engineering in 2000, and the Ph.D. degree in 2005 from the University “Mediterranea” of Reggio Calabria, Italy. Since 2002, he joined the Department of Electronics, Computer Science and Systems at the University of Calabria as Research Associate and, starting from 2006, as Assistant Professor of Electronics. In the summer of 2004, he was Visiting Ph.D. Student at the University of Rochester, New York, USA. His main research interests include the modeling and the optimized design of CMOS high-performance, low-power and ultra low-power digital circuits, design for variability-tolerant and FPGA-based design of image and video processing circuits. He has coauthored about 40 papers published in peer-reviewed international journals and conference proceedings. He has served as technical program committee member for various international conferences and as reviewer for many international journals and conferences.