Fast and Wide Range Voltage Conversion in Multisupply Voltage Designs

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Abstract—Multisupply voltage design technique is widely used in modern system-on-chips to tradeoff energy and speed. Level shifters (LSs) allow different voltage domains to be interfaced. In this brief, a new LS is presented for fast and wide range voltage conversion. Because of a novel architecture combined with the use of multithreshold CMOS technique, the proposed circuit guarantees robust voltage shifting from the deep subthreshold to the above-threshold domain while exhibiting fast response and low energy consumption. When implemented in a 90-nm technology node, considering process-voltage-temperature variations, the proposed design reliably converts 100-mV input signals into 1-V output signals. Post-layout simulation results demonstrate that the new LS shows a propagation delay of 16.6 ns, a static power dissipation of 8.7 nW and a total energy per transition of only 77 fJ for a 0.2 V 1-MHz input pulse.

Index Terms—Level shifter (LS), multisupply voltage design (MSVD), subthreshold operation, ultralow power.

I. INTRODUCTION

Multisupply voltage domain (MSVD) technique is emerging as an effective method to reduce both dynamic and leakage powers in today’s system-on-chips [1]. This approach consists of partitioning the design into separate voltage domains (or voltage islands), each operating at a proper power supply voltage level depending on its timing requirements. Time critical domains run at higher power supply voltage (VDDH) to maximize the performance, whereas non-critical sections work at lower power supply voltage (VDDL), so that dynamic and static power can be reduced without impacting on the overall circuit performance. For extremely low-power applications, the presence of circuit sections operating in subthreshold regime is a valuable option [2]–[4].

In an MSVD system, level shifters (LSs) are required on the boundaries between the circuit subsections operating at different power supply voltages to up-convert signals from the VDDL to the VDDH voltage level [5]. A well-known LS is the differential cascade voltage switch (DCVS) circuit that is typically used for converting signals between the two different above-threshold voltage domains [2]. Unfortunately, the DCVS-LS behaves as a ratioed circuit and the contention between the pull-up and pull-down networks becomes severe when input signals are in the subthreshold range, thus making the conventional sizing techniques impractical to obtain a properly functioning circuit [6]. To address this problem, several improvements to the conventional DCVS circuit have been proposed in [2], [3], and [6]–[10].

The four-stage cascaded DCVS circuit described in [3] assures robust level up-conversion from the subthreshold regime. Unfortunately, it introduces large power penalties, owing to the intermediate power supplies. Furthermore, it shows a limited speed performance. A two-stage LS was proposed in [7]: the first stage exploits a DCVS circuit with an always-on diode-connected nMOS transistor on the top; whereas, the second one is a conventional DCVS stage that achieves rail to rail swing. Such a strategy avoids intermediate power lines, but again it is not enough to reach high speed performances.

The LS proposed in [2] uses two pMOS current limiters to reduce the half-latch pull-up strength within the conventional DCVS structure. In this way, the circuit is able to convert subthreshold input signals and it requires reasonably sized pull-down transistors. Also this LS is relatively slow and energy hungry [6]. A circuit based on current mirrors has been proposed in [6]. It is characterized by significantly better speed performance, but unfortunately, the current mirror output floats when the input voltage signal is high. This causes a significant detrimental effect on subthreshold leakage of the output buffer.

Recently, we proposed a low-power LS, suitable for voltage signal up-conversion from the near/subthreshold regime, which exhibits a very low static and dynamic energy consumption [10]. This is obtained at the expense of reduced voltage conversion range, and of relatively limited speed. In this brief, we present a new LS that trades a certain amount of static power for a significantly improved operating speed and an extended voltage conversion range.

When implemented with the 90-nm ST Microelectronics CMOS technology, the new design reliably converts input signals as low as 0.1 V to the 1 V nominal output voltage, with a delay of ~170 ns.

The remainder of this brief is organized as follows. The proposed design is described in Section II, simulation results and comparison with previously published competitors is provided in Section III; finally, the conclusion is drawn.

II. PROPOSED DESIGN

The proposed LS circuit is shown in Fig. 1. It combines the multithreshold CMOS design technique along with novel topological strategies. The circuit consists of an input inverter, a main voltage conversion stage and an output inverting buffer. The input inverter (MP1/MN1) is designed using low threshold voltage (lvt) transistors. This provides fast differential low-voltage input signals to the main voltage conversion stage [10]. To have higher strength of the pull-down network, also MN2 and MN3 are lvt transistors. Then, two lvt pMOS devices (MP2 and MP3) are added to both the branches of the circuit.

These devices limit the cross-bar current [11] that is the current flowing in the pull-up network and opposing to the discharge of
The above described self-adapting behavior of the pMOS pull-up networks allows managing the contention on critical switching nodes (i.e., NH and NL) in more effective way with respect to [7] and [10], where the action of the pull-up networks is always weakened by the presence of diode-connected transistors. This means that, with respect to the circuit in [10], either smaller nMOS pull-down devices can be used, or equivalently, lower voltage input signals can be successfully up-converted without resizing the nMOS devices. The last option has been chosen in this brief.

It is worth noting that, the use of diode-connected pMOS transistors MP6 and MP7 limits the output range of the main conversion stage to [0 V, VDDH − Vdsat]. To assure a rail-to-rail conversion, an output inverting buffer is connected to the node NH. This inverter uses a standard threshold voltage (svt) nMOS (MN4) device and two stacked hvt pMOS transistors (MP8 and MP9). The used pull-up configuration [12] allows static current when NH is high to be significantly reduced. In such a condition, the MP9 device has the effect of maintaining the source node of MP8 below VDDH. As the source terminal of MP8 results to be at lower voltage than its bulk node, the MP8 threshold voltage increases.

The source-gate voltage of MP8 is also reduced, thus further reducing static current in the above referred condition.

The proposed LS was designed using the 90-nm ST Microelectronics CMOS technology and the transistors were sized, as shown in Table I. For comparison purpose, the circuit has been sized to achieve the minimum energy delay product in the following operating condition: VDDH = 1 V, VDDL = 0.2 V, 100 fF load capacitance on the output node, $T = 25^\circ \text{C}$, TT process corner. It is worth noting that, to reduce the subthreshold leakage current, devices with channel length of 0.20 µm (i.e., twice the minimum channel length allowed in the chosen technology) were used in the main voltage conversion stage and the output inverter. On the contrary, since the leakage current is a minor issue for the input inverter, it exploits devices with minimum channel length, thus enhancing its speed. pMOS transistors in the main voltage conversion stage were sized to further provide a similar falling and rising delay. The right branch of the main voltage conversion stage is downsized with respect to the left one because of the reduced load at the node NL.

In Fig. 3, the physical design of the proposed LS is illustrated. It has been designed according the double-cell-height layout strategy described in [13]. Power supplies are available through the top and the bottom metal-1 rails, while a shared ground rail travels at the center of the cell. The width of the ground rail is twice the width of

**Fig. 2. Transient behavior of the proposed LS.**

**Fig. 3. Layout of the proposed LS.**
the other rails to have consistent abutment with neighboring single-height standard cells.

III. RESULTS AND DISCUSSION

The Cadence Spectre tool was employed for the postlayout analysis. Simulations for three process-voltage-temperature (PVT) corners were performed considering an input signal frequency of 1 MHz, input signal rise- and fall-time of 10 ns and 100 fF of capacitive load.

The typical case corner involves typical n and pMOS transistors, 1 V high supply voltage and a temperature of 25 °C. The second PVT corner was determined considering the worst case operating condition occurring when input signal is in the subthreshold regime. In such a condition, the weakly driven pull-down nMOS transistors have to overpower the corresponding pull-up pMOS devices. Thus, slow-nMOS and fast-pMOS devices are used with a power supply voltage higher than nominal (VDDH = 1.1 V) that further worsens the contention between pull-up and pull-down at NH and NL nodes. Finally, a temperature of −25 °C was used because it implies weaker transistors operation in the subthreshold region. As opposite PVT corner fast-nMOS, slow-pMOS, VDDH = 0.9 V and a temperature of 125 °C were assumed.

In Fig. 4, the worst case propagation delay as a function of the VDDL, for all the analyzed PVT corners, is illustrated. For the TT, 1 V, 25 °C PVT corner, the propagation delay is ∼170 ns, when VDDL = 0.1 V.

Fig. 5 shows the average energy dissipated per transition as a function of VDDL, when an input signal with a frequency of 1 MHz is assumed. The average static power consumption versus VDDL is reported in the same figure. The average energy per transition shows a relatively wide flat energy minimum (for VDDL ranging from 200 to 500 mV). Then, it increases for VDDL lower than 180 mV because short circuit effects become dominant. The static power consumption ranges from 8.6 nW (at VDDL = 100 mV) to 13.2 nW (at VDDL = 0.75 V).

The proposed design was also characterized in terms of worst case delay, taking both interdie and intradie variations into account. To do this, 10,000 run of Monte Carlo (MC) simulations were performed and obtained results are summarized in Fig. 6. A mean delay of 18.2 ns has been obtained, with a standard deviation of 4.4 ns.

In Fig. 7, the distribution of the static current obtained through 1000 run MC simulations is illustrated. It is worth noting that even though the NH voltage does not reach the VDDH voltage level, the static current of the final inverter stage driven by the NH signal does not increase abnormally due to process variability effects.

In Fig. 8, the distribution of the minimum VDDL obtained through 1000 run MC simulations is depicted for the FS 125 °C (a), TT 25 °C (b) and SF −25 °C (c) corners, respectively. In accord with [7], it is determined as the lowest input voltage that allows an output transition toward the VDDH = 1 V to be successfully operated. Results show that the proposed circuit supports reliable level up-conversion from the worst case of 100 mV, occurring at the SF −25 °C corner.

The offset voltage of the main conversion stage could be a concern due to the asymmetrical design. Purpose-performed simulations have shown that, under process variations, when VDDL is set to 100 mV, for the FS 125 °C, TT 25 °C, and SF −25 °C corners, the offset voltage is 12.5, 26, and 30 mV, respectively. That is, it is always lower than the minimum voltage levels that activate an up-conversion.
as shown in Fig. 8. A preliminary comparison done referring to data reported in the original papers shows that the LS circuits presented in [2] and [6] used to up-convert from 100 mV, exhibit a delay of \(\sim\) 500 ns and \(\sim\) 10 \(\mu\)s for the TT, 1 V, 25 °C and the SF, 1.1 V, -25 °C PVT corners, respectively. As shown in Fig. 4, the proposed circuit achieves a delay more than 60% lower. Furthermore, MC simulation results reported in Fig. 6 demonstrates that the new LS reaches a mean delay about 21% and 24% lower than [6] and [10], respectively, with a delay standard deviation \(\sim\) 33% and \(\sim\) 21% lower.

Table II shows the characteristics of the new LS and those of previously proposed designs. The table is divided in two portions. The first one reports the results from original papers obtained by measurements on the fabricated prototypes [2], [7], [9], [14]. The second portion is related to circuits replicated in this brief [2], [6], [8], [10]. For the sake of comparison, those circuits have been sized to achieve the minimum energy delay product and they were laid-out using the 90-nm ST Microelectronics CMOS technology and the above-mentioned layout strategy. It should be noted that the circuit in [2] has been realized considering the sizing criterion suggested in [6]. Furthermore, based on the results shown in [14], the current mirror-based circuit presented in [6] has been laid out including the output buffer designed as suggested in the original brief.

From Table II, it can be observed that the LS proposed in [14] realized using a 0.35-\(\mu\)m process exhibits quite low power consumption. Unfortunately, this is obtained at the expense of a very high delay. The LS circuit presented in [2] has been fabricated using a 0.13-\(\mu\)m process. It shows a relatively good speed performance, but its power dissipation is quite high.

Among the circuits compared at a parity of technology node, it can be observed that the circuits proposed in [8], exhibit the highest speed. This is mainly due to the use of the DTMOS technique. However, their power dissipation is about three orders of magnitude higher than their power dissipation is about three orders of magnitude higher than competitors. Moreover, the circuit proposed in [2] shows the highest delay. Whereas, the LS demonstrated in [6] exhibits a relatively low delay and average energy per transition. Unfortunately, since the output node of the current mirror floats when the input voltage signal is high, a detrimental effect on the subthreshold leakage of the output buffer occurs. This leads to a large static power dissipation of the whole LS architecture (20.4 nW at 0.2 V).

The LS presented in [10], exhibits the lowest static power dissipation and energy per transition with a delay of 23.5 ns at 0.2 V. However, it up-converts input voltage as low as 0.18 V.

The design proposed here improves the operation speed of about 29% with respect to [10], while consuming only 13% more energy per transition, but extending the operative voltage conversion range down to 0.1 V.

**IV. CONCLUSION**

A new LS suitable for robust logic voltage shifting from near/subthreshold to above-threshold domain has been presented. The proposed circuit exploits proper design strategies to increase the operating speed while maintaining very low energy consumption and large voltage conversion range. When used to up-convert voltage signals from the deep subthreshold regime, the novel design outperforms all the previously proposed LSs.

**REFERENCES**


