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Gate-level body biasing technique for high-speed sub-threshold CMOS logic gates

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An efficient technique for designing high-performance logic circuits operating in sub-threshold region is proposed. A simple gate-level body biasing circuit is exploited to change dynamically the threshold voltage of transistors on the basis of the gate status. Such an auxiliary circuit prepares the logic gate for fast switching while maintaining energy efficiency.

If 200 aJ is the target total energy per operation consumption, a two input NAND (NOR) gate designed as described here shows a delay reduction between 20% (16%) and 40% (48%), with respect to previously proposed sub-threshold approaches. Copyright 2012 John Wiley & Sons, Ltd.

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1. INTRODUCTION

Ultra-low energy digital complementary metal–oxide–semiconductor (CMOS) circuits are rapidly gaining a wide interest due to the large proliferation of battery-powered electronic devices [1]. Power supply voltage (V_{dd}) scaling below the transistor threshold voltage (V_{th}) is one of the most effective approaches to achieve low-energy consumption. However, energy saving is obtained at the expense of reduced computational speed [2, 3] and increased sensitivity to temperature and process variations [2, 4].While acceptable for niche markets, such as wristwatches and hearing aids, the delay penalty can be very limitative for a broader set of applications [5].

In order to improve the speed performance of sub-threshold circuits, the forward body biasing technique is widely adopted [2, 6]. Such strategy also allows minimizing the effects of process and temperature variations, while maintaining energy efficiency [6]. Furthermore, the combination of forward body biasing with steep retrograde channel doping profile has the potential to extend the scalability of the bulk-Si metal–oxide–semiconductor field-effect transistor (MOSFET) technology down to 10 nm transistor channel length [7].

This letter demonstrates a body bias driven design methodology to achieve easily fast, energy efficient and robust sub-threshold CMOS logic gates.

2. SUB-THRESHOLD LOGIC DESIGN

In Figure 1, several NMOS transistor configurations commonly used in the design of pull-down networks (PDNs) of sub-threshold CMOS static logic gates are illustrated. Figure 1a shows the standard MOSFET, Figure 1b depicts the traditional dynamic threshold MOS (DTMOS) configuration [2], whereas

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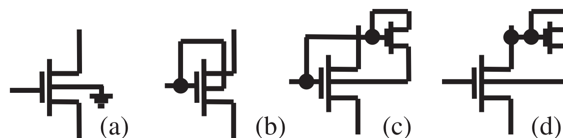

Figure 1. Sub-threshold transistor configurations: a) conventional MOSFET; b) DTMOS; c) DTMOS_1; d) DTMOS_2.

Figures 1c and 1d show more recent variants of the DTMOS style [8, 9], here called DTMOS_1 and DTMOS_2. Pull-up networks (PUNs) are designed exploiting similarly organized PMOS transistors.

The DTMOS technique (Figure 1b) improves speed-performance, with respect to standard CMOS using transistors with gates tied to their substrates. As the substrate voltage varies with the input gate voltage V_{in}, the threshold voltage is dynamically changed [2]. When $V_{in} = V_{dd}$ ($V_{in} = 0\,\mathrm{V}$), the substrate-source junction of the NMOS (PMOS) transistor is forward-biased and thus the threshold voltage is reduced [2]. This leads to higher ON current causing DTMOS transistors to switch faster than conventional MOSFETs. As a drawback, this configuration implies input capacitances significantly larger than a standard CMOS gate [8]. This counteracts its intrinsic speed advantages. To reduce the above effect, configurations DTMOS_1 and DTMOS_2 can be used [8, 9]. Furthermore, it should be noted that the substrate bias voltage of DTMOS gates would change also when input transitions do not imply output switching. This would charge and discharge the large body capacitances, thus wasting precious energy.

3. PROPOSED DESIGN TECHNIQUE

Different from the transistor-level approaches above discussed, the technique proposed here and schematized in Figure. 2 is based on a gate-level body biasing scheme.

The PUN and PDN substrates voltage *V_Bulk* is generated dynamically by the built-in body biasing generator (BBG), depending on the logic gate status. The BBG transfers the output voltage signal to the PUN and PDN substrates decoupling the large body capacitances from the output node. When the output voltage is 0 V, the PMOS in the BBG transfers a low voltage on the *V_Bulk* net, preparing the PUN for a faster transition. On the contrary, if the output voltage is V_{dd}, then a high voltage is transferred through the NMOS to the substrates thus allowing the PDN to switch faster. In both cases, the MOSFETs in the switching network are already forward body biased before input arrivals, allowing instantaneous higher current to flow through the switching transistors. This extra current is then rapidly suppressed after the output voltage is changed, and the BBG allows forward

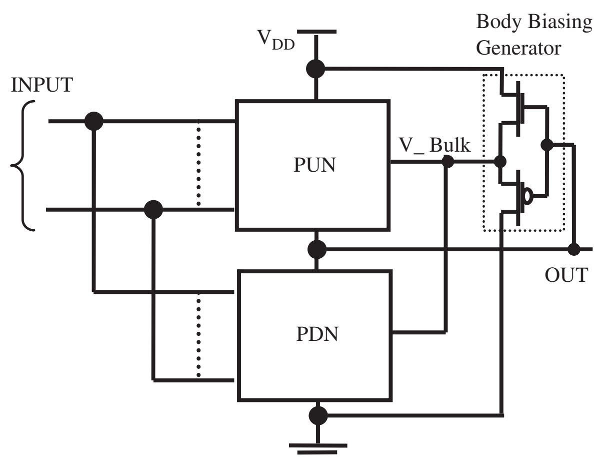

Figure 2. The proposed technique.

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body biasing to be set for accelerating the subsequent output logic transition. The BBG transistors can be downsized, thus minimizing their capacitive effects on the output node of the logic gate. On the other side, the quite high capacitive load seen by the BBG does not constitute a bottleneck. In fact, *V_Bulk* is established by an output transition to provide fast switching in the subsequent gate transition.

Logic gates designed as proposed here exhibit further performance and energy advantages over the DTMOS solutions due to their reduced input capacitances that equal those of the standard MOSFET configuration. Finally, when input signals switch without changing the gate output voltage, the BBG does not waste energy by charging/discharging the body capacitances.

The intrinsic speed improvement of the proposed design technique is obtained at the expense of a somewhat increased leakage current flowing through the OFF network (either PUN or PDN) during the gate idle status.

However, the impact of leakage currents on total energy dissipation strictly depends on the activity cycle time of the implemented circuit; provided that all low-power devices are usually placed in sleep-mode during long stand-by. Our target is the efficient implementation of core processors, such as ARM™ Cortex, iCORE™, Lexra™ and Xtensa™, whose clock cycle time is ≈ 50 FO4, on average; FO4 being the delay of a CMOS inverter driving four identical inverters. For these reasons, all experiments have been performed under this running condition.

4. RESULTS

Energy and delay characteristics obtained using the proposed approach and its competitors were evaluated considering two-input NAND and NOR gates as benchmarks. All the logic gates were designed using the STMicroelectronics 45 nm 1 V CMOS technology, and they were sized for a fixed ratio of 1.5*W/1*W between PUN and PDN. Auxiliary transistors are minimum sized.

A first set of simulations was performed for V_{dd} = 300 mV, T = 27 °C and a capacitive load of 1.2 fF. All compared circuits were driven with input signals having rise and fall times of ≈ 150 ps. For the chosen technology, the 50 FO4 clock cycle time corresponds to 15 ns @ V_{dd} = 300 mV and T = 27 °C.

Figure 3a illustrates the total energy per operation (E_{op}) versus the delay of the compared NAND gates. The curves have been obtained varying the sizing factor W from 0.12 μm to 1.2 μm, with a step of 0.12 μm. The insets help in identifying the minimum size and maximum size points. It is easy to observe that for a given E_{op} constraint, the proposed technique allows the lowest propagation delay to be reached. In Figure 3b, the leakage energy-per-operation (E_{leak}) versus delay curves are depicted. Figures 3c and 3d report analogous results for the compared NOR gates.

From an inspection of the above results, it can be observed that, if the minimum total energy is the target, the minimum size standard CMOS represents the better choice allowing the lowest energy dissipation to be reached. In fact, $E_{leak,\mathrm{NAND}}$ = 10.35 aJ and $E_{op,\mathrm{NAND}}$ = 83 aJ ($E_{leak,\mathrm{NOR}}$ = 10.49 aJ, $E_{op,\mathrm{NOR}}$ = 85 aJ) are obtained for the NAND (NOR) standard CMOS gate. However, the lowest energy dissipation is reached at the expense of switching speed (523 ps for the NAND and 822 ps for the NOR). On the contrary, when the speed requirement is more stringent, the new style becomes the only reasonable choice: the NAND (NOR) gate designed as proposed here exhibits a delay lower than 266 ps (376 ps) with the lowest E_{op} and E_{leak}. Furthermore, the delay ranges of 195 ps-243 ps and 270 ps-333 ps achieved for the NAND and the NOR, respectively, are unaffordable for all previously known NAND and NOR configurations. From Figures 3b and 3d, it can be observed that at a parity of transistor sizes, the DTMOS_2 and the proposed technique show leakage higher than other competitors. However, this does not represent a real drawback of the new design approach because, as above explained, it allows either the energy or the delay target to be reached using smaller transistors.

To extend the analysis, simulations were carried out cascading three identical logic gates. In this way, the effects of the input and output capacitances are fully taken into account. For comparison purposes, all compared gates were sized to have similar leakage E_{op} consumption.

In Figures 4a and 4b, the delay and the E_{op} of the NAND chains are plotted versus the temperature. Similar results are provided for the NOR chains in Figures 4c and 4d. It can be easily seen that energy

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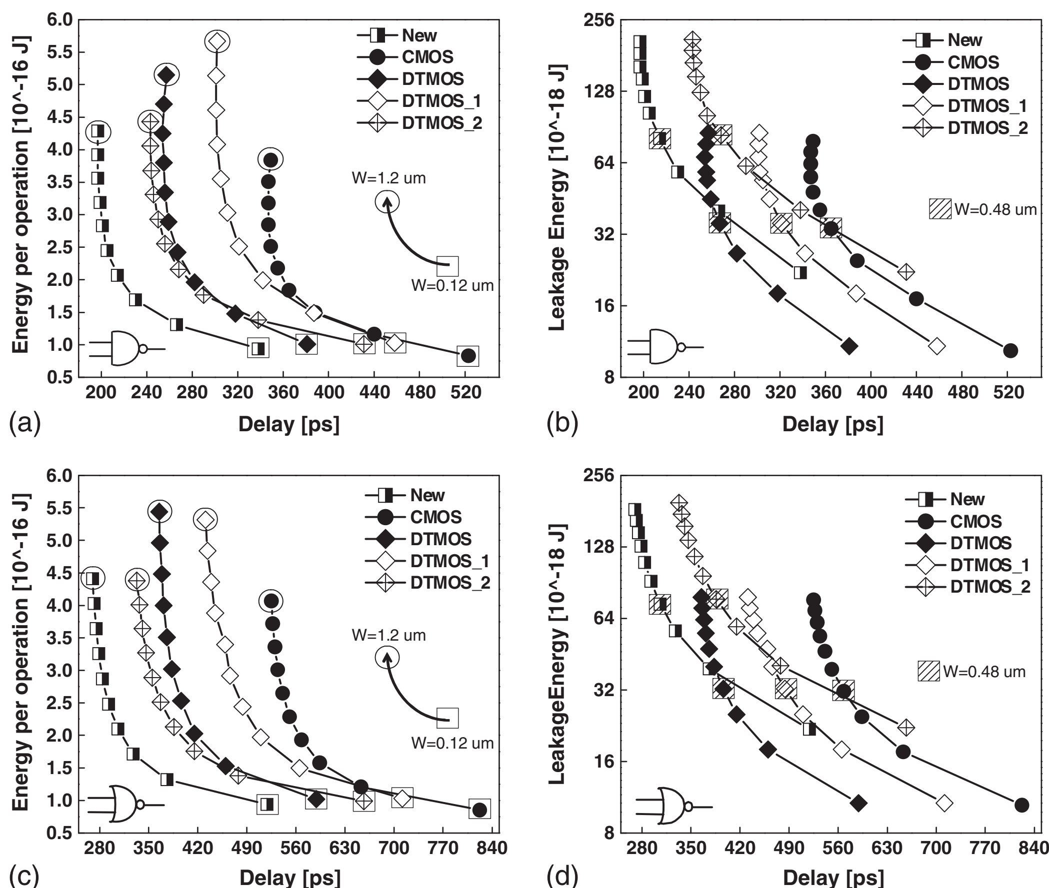

Figure 3. Simulation results (log2 scale): a) Energy per operation-delay plots - NAND gates. b) Leakage energy plots - NAND gates. c) Energy per operation-delay plots - NOR gates. d) Leakage energy plots - NOR gates.

and delay advantages offered by the novel approach are maintained over the temperature range. As the temperature increases from the nominal value of 25 °C up to 100 °C, both the DTMOS_2 and the proposed implementations show very similar energy degradation trends. Differently, the DTMOS_1-based circuits show larger energy sensitivity against temperature fluctuations.

Table I shows the leakage currents of the overall analyzed circuits for several temperature values. Due to the adopted sizing criterion, all the circuits show similar leakage currents at low operating temperatures. As the temperature increases, the proposed technique proves a slightly better behavior. This is mainly due to the smaller transistor devices.

The last set of simulations was aimed to investigate the impact of process variability, evaluated through 1000 samples Monte Carlo simulations performed on the NAND and NOR chains. In this analysis, both inter-die and intra-die fluctuations were considered. Mean (μ) and standard deviation (σ) values of delay and energy are collected in Table II.

It can be observed that the proposed design style achieves the lowest mean values for both delay and energy. In most cases, the new technique overcomes competitors also in terms of standard deviation. Considering the well-known 3-sigma rule, it can be claimed that the 99.7% of samples of the new designed NAND chain will reach a delay lower than 1.53 ns (i.e. $\mu_{\text{Delay}} + 3\sigma_{\text{Delay}}$) and will dissipate less than 0.995fJ (i.e. $\mu_{\text{Energy}} + 3\sigma_{\text{Energy}}$). This leads to an energy-delay-product of ~1.52 ns*fJ. The most competitive alternative (i.e. DTMOS_2) can achieve an energy-delay-product of ~1.73 ns*fJ, which is ~39.5% higher.

The statistical analysis of the NOR gate has given even better results. The circuit designed as proposed here exhibits an energy-delay-product of ~5.9 ns*fJ, whereas the best competitor (i.e. DTMOS_1) reaches ~15.75 ns*fJ.

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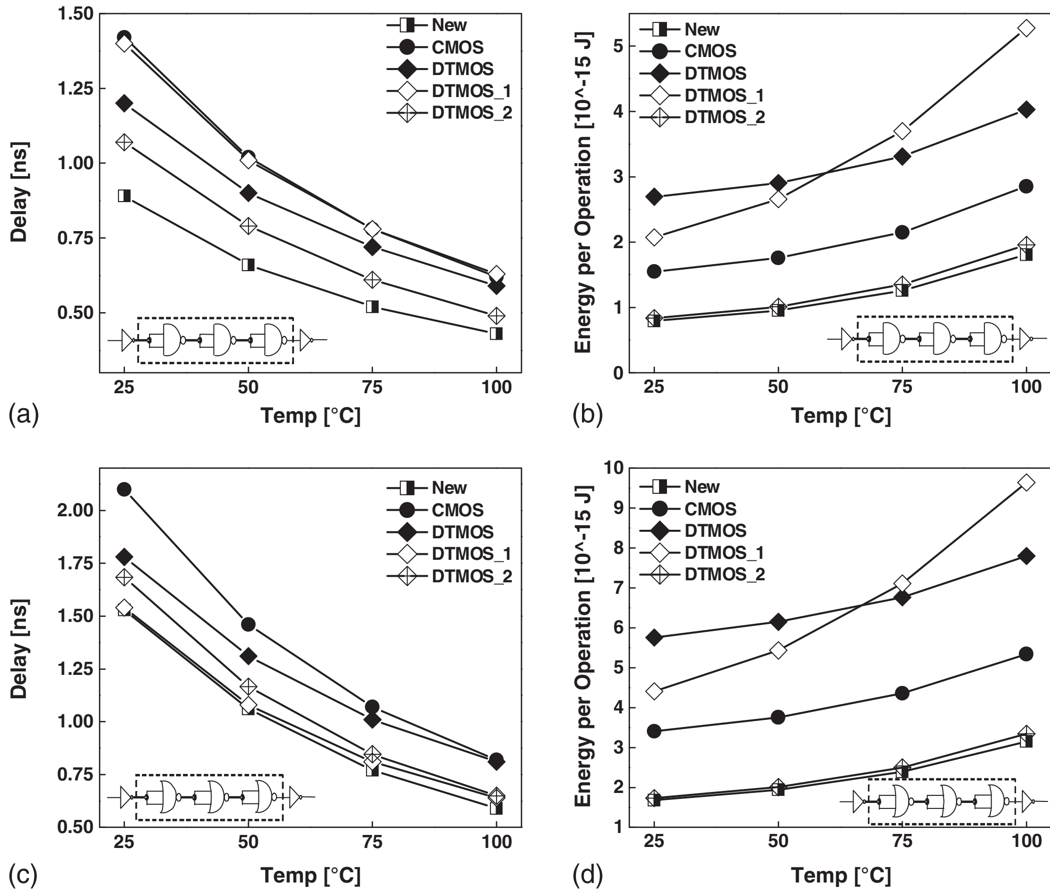

Figure 4. Temperature variation results. All NAND (NOR) gates are sized for similar leakage energy $E_{leak} \approx 58$ aJ ($E_{leak} \approx 60$ aJ). a) Delay versus temperature for NAND chains; b) Energy versus temperature for NAND chains; c) Delay versus temperature for NOR chains; d) Energy versus temperature for NOR chains.

Table I. Leakage current versus temperature results.

	Temp [°C]	NEW	CMOS	DTMOS	DTMOS_1	DTMOS_2
NAND chain	25	31.19 nA	29.90 nA	29.88 nA	29.88 nA	31.60 nA
	50	73.50 nA	73.20 nA	73.24 nA	73.24 nA	74.60 nA
	75	154.30 nA	161.20 nA	161.30 nA	161.30 nA	156.70 nA
	100	293.40 nA	320.80 nA	321.40 nA	321.40 nA	297.30 nA
NOR chain	25	29.16 nA	28.83 nA	28.8 nA	28.8 nA	30.7 nA
	50	62.14 nA	62.91 nA	62.89 nA	62.89 nA	64.41 nA
	75	121.11 nA	127.3 nA	127.3 nA	127.3 nA	126.6 nA
	100	217.99 nA	238 nA	238.8 nA	238.8 nA	219.2 nA

Table II. Monte Carlo results (@V_{dd} = 300 mV. T = 27 °C. Tcycle = 50 FO4).

	Performance parameters		NEW	CMOS	DTMOS	DTMOS_1	DTMOS_2
NAND chain	**Delay**	μ [ns]	0.9	1.4	1.2	1.4	1.1
		σ [ps]	209	366	239	347	259
	Energy	μ [fJ]	0.8	1.6	2.7	2.2	0.9
		σ [aJ]	65	88	96	216	76
NOR chain	**Delay**	μ [ns]	1.5	2.1	1.8	1.5	1.7
		σ [ps]	455	603	411	401	526
	Energy	μ [fJ]	1.7	3.5	5.8	4.6	1.8
		σ [aJ]	120	150	180	409	145

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5. CONCLUSION

A novel technique to design efficient logic gates in sub-threshold regime is proposed. Experimental results demonstrate higher performance and lower total energy consumption with respect to the previous proposed approaches. Moreover, higher tolerance to process variations is guaranteed.

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